

Topological index calculation of DAEs in circuit simulation

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Abstract. Electric circuits are present in several applications, e.g. in home computers, television, credit cards, electric power networks, etc. The development of integrated circuit requires numerical simulation. Modern modeling techniques like the Modified Nodal Analysis (MNA) lead to differential algebraic equations (DAEs). The analytical and numerical solutions of these systems depend strongly on the structure and the index.

The paper deals with lumped circuits containing voltage sources, current sources as well as general nonlinear but time-invariant capacitances, inductances and resistances. We present network-topological criteria for the index of the DAEs obtained by the classical and the charge oriented MNA. Furthermore, the index is shown to be limited to 2 for the considered model-class.

Key words. Circuit simulation, integrated circuit, differential-algebraic equation, DAE, index, modified nodal analysis, MNA

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1 Basics of electric circuit analysis

Consider lumped electric circuits containing resistances, capacitances, inductances, voltage sources and current sources. For two-terminal (one-port) lumped elements, the current through the element and the voltage across it are well-defined quantities. For lumped elements with more than two terminals, the current entering any terminal and the voltage across any pair of terminals are well defined at all times (cf. [2]). Hence, general time-invariant n -terminal resistances can be modeled by an equation system of the form

$$j_k = g_k^e(u_1, \dots, u_{n-1}) \quad \text{for } k = 1, \dots, n-1$$

if j_k represents the current entering terminal k and u_l describes the voltage across the pair of terminals $\{l, n\}$ (for $k, l = 1, \dots, n-1$). In this case, we call the terminal n the reference terminal. The Kirchhoff's Current Law implies the current entering terminal n to be given by $j_n = -\sum_{k=1}^{n-1} j_k$. The conductance matrix $G^e(u_1, \dots, u_{n-1})$ is defined by the Jacobian

$$G^e(u_1, \dots, u_{n-1}) := \begin{pmatrix} \frac{\partial g_1^e}{\partial u_1} & \cdots & \frac{\partial g_1^e}{\partial u_{n-1}} \\ \vdots & \ddots & \vdots \\ \frac{\partial g_{n-1}^e}{\partial u_1} & \cdots & \frac{\partial g_{n-1}^e}{\partial u_{n-1}} \end{pmatrix}.$$

The index e shall specify the correlation to a special element of a circuit. Later on we will introduce the conductance matrix $G(u)$ describing all resistances of a circuit. Correspondingly, the capacitance matrix $C^e(v_1, \dots, v_{n-1})$ of a general nonlinear n -terminal capacitance is given by

$$C^e(u_1, \dots, u_{n-1}) := \begin{pmatrix} \frac{\partial q_1^e}{\partial u_1} & \cdots & \frac{\partial q_1^e}{\partial u_{n-1}} \\ \vdots & \ddots & \vdots \\ \frac{\partial q_{n-1}^e}{\partial u_1} & \cdots & \frac{\partial q_{n-1}^e}{\partial u_{n-1}} \end{pmatrix}$$

if the voltage-current relation is defined by means of charges by

$$j_k = \frac{d}{dt} q_k^e(u_1, \dots, u_{n-1}) \quad \text{for } k = 1, \dots, n-1.$$

Inductances can be modeled by means of fluxes by

$$u_k = \frac{d}{dt} \phi_k^e(j_1, \dots, j_{n-1}) \quad \text{for } k = 1, \dots, n-1.$$

Then, the inductance matrix $L^e(j_1, \dots, j_{n-1})$ is given by the Jacobian

$$L^e(j_1, \dots, j_{n-1}) := \begin{pmatrix} \frac{\partial \phi_1^e}{\partial j_1} & \cdots & \frac{\partial \phi_1^e}{\partial j_{n-1}} \\ \vdots & \ddots & \vdots \\ \frac{\partial \phi_{n-1}^e}{\partial j_1} & \cdots & \frac{\partial \phi_{n-1}^e}{\partial j_{n-1}} \end{pmatrix}.$$

Assume all voltage and current sources to be *independent* sources for a while. At the end of the paper we will generalize the main results for some controlled sources.

One of the most commonly used network analyses in circuit simulation is the Modified Node Analysis (MNA). It represents a systematic treatment of general circuits and is important when computers perform the analysis of networks automatically. For the MNA the vector of unknowns consists of all node voltages and all branch currents of current controlled elements. Performing the MNA means:

1. Write node equations by applying KCL (Kirchhoff's Current Law) to each node except for the datum node:

$$Aj = 0. \tag{1}$$

The vector j represents the branch current vector. The matrix A is called the (reduced) incidence matrix and describes the network graph, the branch-node relations. Moreover, it holds

$$a_{ik} = \begin{cases} 1 & \text{if branch } k \text{ leaves node } i \\ -1 & \text{if branch } k \text{ enters node } i \\ 0 & \text{if branch } k \text{ is not incident with node } i \end{cases}$$

for the elements of A .

2. Replace the currents j_k of voltage controlled elements by the voltage-current relation of these elements in equation (1).
3. Add the current-voltage relations for all current controlled elements.

Note, in case of multi-terminal elements with n terminals we speak of branches if they represent a pair of terminals $\{l, n\}$ with $1 \leq l \leq n - 1$.

In general, the MNA leads to a coupled system of implicit differential equations and nonlinear equations, i.e. to a quasilinear differential-algebraic equation (DAE)

$$A(x)\dot{x} + f(x) = s(t) \quad (2)$$

(cf. [9] in this journal). The analytical and numerical solutions of (2) depend strongly on its structure and on its index. For a detailed discussion of this fact we refer to [9] in this journal, [7] and [14]. In this article we analyze the structure of the DAEs obtained by the MNA in more detail. This implies important information about sensitivity and transient behavior of solutions.

Split the incidence matrix A into the element-related incidence matrices $A = (A_C A_L A_R A_V A_I)$, where A_C , A_L , A_R , A_V and A_I describe the branch-current relation for capacitive branches, inductive branches, resistive branches, branches of voltage sources and branches of current sources, respectively. Denote by e the node potentials (excepting the datum node) and by j_L and j_V the current vectors of inductances and voltage sources. Defining by i and v the vector of time-dependent functions for current and voltage sources, respectively, we obtain the following equation system from the MNA:

$$A_C \frac{dq(A_C^T e)}{dt} + A_R g(A_R^T e) + A_L j_L + A_V j_V + A_I i = 0, \quad (3)$$

$$\frac{d\phi(j_L)}{dt} - A_L^T e = 0, \quad (4)$$

$$A_V^T e - v = 0. \quad (5)$$

The splitting of the incidence matrix A corresponding to certain branches leads to the following useful structural information for lumped circuits:

Theorem 1.1 *Given a lumped circuit with the (reduced) incidence matrix $A = (A_C A_L A_R A_V A_I)$, the following relations are satisfied.*

1. *The matrix $(A_C A_L A_R A_V)$ has full row rank.*
2. *The matrix A_V has full column rank.*
3. *The matrix $(A_C A_R A_V)$ has full row rank if and only if the circuit does not contain a cut-set consisting of inductances and/or current sources only.*
4. *Let Q_C be any projector onto $\ker A_C$. Then, the matrix $Q_C^T A_V$ has full column rank if and only if the circuit does not contain a loop consisting of capacitances and voltage sources only.*

Note, loops containing only capacitances are excluded under point 4 whereas cut-sets containing only inductances are included under point 3 of Theorem 1.1.

Proof:

1. The Kirchhoff's Current Law implies that the network can not contain cut-sets formed only by current sources. Hence, there is a tree consisting of capacitive, inductive, resistive and voltage source branches (cf. [2]). The columns of $(A_C A_L A_R A_V)$, corresponding to this tree, are linear independent, i.e. $\text{rank}(A_C A_L A_R A_V) = N - 1$ (here N denotes the number of nodes of the circuit).
2. The Kirchhoff's Voltage Law implies that the network can not contain loops formed only by voltage sources. This means, that the columns of A_V are linear independent.
3. The matrix $(A_C A_R A_V)$ has full row rank if and only if it has $N - 1$ linear independent columns. This is equivalent to the fact that there is a tree of the circuit that contains capacitive, resistive and voltage source branches only. But this means exactly, that the circuit does not contain a cut-set consisting of inductances and/or current sources only.
4. Firstly, assume there is a loop, consisting of capacitances and voltage sources only. Then it is easy to verify, that the columns of the matrix $(A_V A_C)$ are linear dependent. Therefore, we find a nontrivial vector $\begin{pmatrix} x \\ y \end{pmatrix}$ (corresponding to the considered loop) such that $(A_V A_C) \begin{pmatrix} x \\ y \end{pmatrix} = 0$. Multiplying this equation with Q_C^T we get $Q_C^T A_V x = 0$. The assumption $x = 0$ would imply $A_C y = 0$, i.e. the considered loop would be a loop consisting of capacitances only, that we have excluded. Hence $x \neq 0$, i.e. $\ker Q_C^T A_V \neq \{0\}$.
Secondly, assume there is a nontrivial x such that $Q_C^T A_V x = 0$. Then $A_V x \in \ker Q_C^T = \text{im } A_C$, i.e. there is a y such that $A_V x + A_C y = 0$. Since $x \neq 0$, there is a loop consisting of capacitances and voltage sources.

q.e.d.

In the following section the special cut-sets and loops considered in Theorem 1.1 will be important. Therefore we define:

1. A **L-I cut-set** is a cut-set consisting of inductances and/or current sources only.
2. A **C-V loop** is a loop, consisting of capacitances and voltage sources only.

2 DAE index of the network equations

The solution behavior of DAEs depends strongly on the index of DAEs. Generally, numerical difficulties increase with higher index, since numerical differentiation is an unstable procedure (see e.g. [1], [10], [12]). There are different index concepts extending the Kronecker-Index (for linear DAEs) to nonlinear DAEs. The differential index ([1]) is perhaps the one that is most often used in practical applications, because it is easy to determine for a special given problem. In this article, we investigate the tractability index ([12]) for circuit systems in order to apply interesting results about solvability and stability for

index-1-tractable and index-2-tractable DAEs. Furthermore, this index concept requires only weak smoothness conditions that are important for circuit simulation.

1. The DAE (2) is called index-1-tractable if the matrix $A_1(x) := A(x) + f'_x(x)Q$ is regular for a projector Q onto the null space of $A(x)$.
2. The DAE (2) is called index-2-tractable if
 - (a) it is not index-1-tractable,
 - (b) $N \cap S(x)$ is of constant rank for $N := \ker A(x)$ and $S(x) := \{z : f'_x(x)z \in \text{im } A(x)\}$,
 - (c) $N_1(x) \cap S_1(x) = \{0\}$ for $N_1(x) := \ker A_1(x)$ and $S_1(x) := \{z : f'_x(x)(I - Q)z \in \text{im } A_1(x)\}$.

Remark: The following results for the tractability index are also satisfied for the differential index. For a proof we refer to [4].

Writing system (3)-(5) as a DAE of form (2) the matrix $A(x)$ reads

$$A(x) = \begin{pmatrix} A_C C(A_C^T e) A_C^T & 0 & 0 \\ 0 & L(j_L) & 0 \\ 0 & 0 & 0 \end{pmatrix}, \quad (6)$$

where $C(u) := \frac{dq(u)}{du}$ and $L(j) := \frac{d\phi(j)}{dj}$. The (mostly nonlinear) function $f(x)$ and the vector function $s(t)$ are given by

$$f(x) = \begin{pmatrix} A_R g(A_R^T e) + A_L j_L + A_V j_V \\ -A_L^T e \\ A_V^T e \end{pmatrix} \quad \text{and} \quad s(t) = \begin{pmatrix} -A_I i(t) \\ 0 \\ v(t) \end{pmatrix}. \quad (7)$$

Before we present criteria for the index of DAEs in circuit simulation, we want to formulate two useful lemmata.

Lemma 2.1 *If the capacitance and inductance matrices of all capacitances and inductances are positive definite then the following relations are satisfied*

$$\ker A(x) = \ker A_C^T \times \{0\} \times \mathbb{R}^{n_V} \quad \text{and} \quad \text{im } A(x) = \text{im } A_C \times \mathbb{R}^{n_L} \times \{0\},$$

where n_L and n_V denote the number of inductance branches and voltage sources, respectively.

Note, Lemma 2.1 implies that the null space $\ker A(x)$ as well as the image space $\text{im } A(x)$ do not depend on x .

Lemma 2.2 *If M is a positive definite $m \times m$ -matrix and N is a rectangular matrix of dimension $k \times m$, then it holds that*

$$\ker NMN^T = \ker N^T \quad \text{and} \quad \text{im } NMN^T = \text{im } N.$$

The correctness of Lemma 2.1 and Lemma 2.2 follows immediately from the definition of positive definite matrices.

Theorem 2.3 *Let the capacitance, inductance and resistance matrices of all capacitances, inductances and resistances, respectively, be positive definite. If the network contains neither L-I cut-sets nor C-V loops, then the MNA leads to an index-1-tractable DAE.*

Remark: If the network contains a loop, consisting of capacitances only, then the *Mesh Analysis* leads to an index higher than 1 since the current through such a loop belongs to the vector of unknowns and represents an index-2 variable. In case of the MNA, the current through such a loop does not belong to the vector of unknowns. This fact makes clear, that the index of a circuit equation system depends also on the scheme for setting up the equations.

Proof of Theorem 2.3: We will show that the DAE (2) is index-1-tractable, i.e. that the matrix $A_1(x)$ is regular. Let Q_C be a constant projector onto $\ker A_C^T$. Regarding Lemma 2.1,

$$Q := \begin{pmatrix} Q_C & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & I \end{pmatrix}$$

represents a constant projector onto $\ker A(x)$. We denote by $G(u) := \frac{dg(u)}{du}$. Then the matrix $A_1(x)$ is given by

$$A_1(x) = \begin{pmatrix} A_C C (A_C^T e) A_C^T + A_R G(A_R^T e) A_R^T Q_C & 0 & A_V \\ -A_L^T Q_C & L(j_L) & 0 \\ A_V^T Q_C & 0 & 0 \end{pmatrix}. \quad (8)$$

If $z = \begin{pmatrix} z_e \\ z_L \\ z_V \end{pmatrix}$ is any vector of the null space of $A_1(x)$, then it holds

$$A_C C (A_C^T e) A_C^T z_e + A_R G(A_R^T e) A_R^T Q_C z_e + A_V z_V = 0, \quad (9)$$

$$-A_L^T Q_C z_e + L(j_L) z_L = 0, \quad (10)$$

$$A_V^T Q_C z_e = 0. \quad (11)$$

Multiplying (9) by Q_C^T we obtain

$$Q_C^T A_R G(A_R^T e) A_R^T Q_C z_e + Q_C^T A_V z_V = 0, \quad (12)$$

since $Q_C^T A_C = 0$. Let Q_{V-C} be a projector onto $\ker A_V^T Q_C$. Multiplying (12) by Q_{V-C}^T yields

$$Q_{V-C}^T Q_C^T A_R G(A_R^T e) A_R^T Q_C z_e = 0. \quad (13)$$

From (11) we know that $z_e \in \ker A_V^T Q_C$, i.e.,

$$z_e = Q_{V-C} z_e. \quad (14)$$

Thus, we may write (13) as

$$Q_{V-C}^T Q_C^T A_R G(A_R^T e) A_R^T Q_C Q_{V-C} z_e = 0.$$

Lemma 2.2 implies $A_R^T Q_C Q_{V-C} z_e = 0$. Applying (14) we get

$$A_R^T Q_C z_e = 0. \quad (15)$$

Adding (11) and (15), we obtain $(A_V A_R A_C)^T Q_C z_e = 0$. Applying Theorem 1.1-3 we may conclude

$$Q_C z_e = 0. \quad (16)$$

since the circuit does not contain an L-I cut-set. Regarding (12) we obtain $Q_C^T A_V z_V = 0$. Applying Theorem 1.1-4 we find out that $z_V = 0$ since the circuit does not contain a C-V loop. Regarding (9) and (16) we deduce

$$A_C C (A_C^T e) A_C^T z_e = 0.$$

Thus, Lemma 2.2 implies $A_C^T z_e = 0$, i.e. z_e belongs to the image space of the projector Q_C . With (16) we conclude that $z_e = Q_C z_e = 0$. Since A_V has full column rank (see Theorem 1.1) and $L(j_L)$ is positive definite, the equations (9) and (10) imply $z_V = 0$ and $z_L = 0$. This means, that the matrix $A_1(x)$ is regular and the circuit equation system has index 1.

q.e.d.

Theorem 2.4 *Let the capacitance, inductance and resistance matrices of all capacitances, inductances and resistances, respectively, be positive definite. If the network contains an L-I cut-set or a C-V loop, then the MNA leads to an index-2-tractable DAE.*

Proof: Choosing the same projectors as in the proof of Theorem 2.3, we construct a non-zero vector belonging to the null space of $A_1(x)$. We consider the two possibilities:

1. The network contains an L-I cut-set. Applying Theorem 1.1-3 we find a nontrivial z_e such that $z_e^T (A_C A_R A_V) = 0$. This implies $z_e = Q_C z_e$ and for $z := \begin{pmatrix} z_e \\ 0 \\ 0 \end{pmatrix}$ holds $A_1(x)z = 0$.
2. The network contains a C-V loop. Applying Theorem 1.1-4 we find a nontrivial z_V such that $Q_C^T A_V z_V = 0$. This implies $A_V z_V = A_C C (A_C^T e) A_C^T z_e$ for a certain $z_e \in \ker Q_C$. Choosing $z := \begin{pmatrix} z_e \\ 0 \\ -z_V \end{pmatrix}$ we obtain $A_1(x)z = 0$.

Next, we remark that the the intersection

$$\ker A \cap S(x) = \{z : A_C^T z_e = 0, A_V^T z_e = 0, A_R G (A_R^T e) A_R^T z_e + A_L z_L + A_V z_V \in \text{im } A_C\}$$

is constant since $G(A_R^T e)$ is positive definite.

It remains to show that $N_1(x) \cap S_1(x) = \{0\}$ is satisfied. Choosing $z = \begin{pmatrix} z_e \\ z_L \\ z_V \end{pmatrix} \in N_1(x) \cap S_1(x)$, regarding (8) and defining $P_C := I - Q_C$ we find α and γ such, that

$$A_C C(A_C^T e) A_C^T z_e + A_R G(A_R^T e) A_R^T Q_C z_e + A_V z_V = 0, \quad (17)$$

$$-A_L^T Q_C z_e + L(j_L) z_L = 0, \quad (18)$$

$$A_V^T Q_C z_e = 0, \quad (19)$$

$$\begin{aligned} A_R G(A_R^T e) A_R^T P_C z_e + A_L z_L &= A_R G(A_R^T e) A_R^T Q_C \alpha \\ &+ A_C C(A_C^T e) A_C^T \alpha + A_V \gamma, \end{aligned} \quad (20)$$

$$A_V^T P_C z_e = A_V^T Q_C \alpha. \quad (21)$$

Multiplying (17) by $Q_{V-C}^T Q_C^T$ (cf. proof of Theorem 2.3-1), regarding (19) and applying Lemma 2.2 we obtain $A_R^T Q_C z_e = 0$. This implies together with (19) that

$$Q_C z_e = Q_{CRV} z_e \quad (22)$$

for a projector Q_{CRV} onto $\ker(A_C A_R A_V)^T$. Multiplying (20) by Q_{CRV}^T and using (18) we obtain

$$0 = Q_{CRV}^T A_L z_L = Q_{CRV}^T A_L L^{-1}(i_L) A_L^T Q_C z_e = Q_{CRV}^T A_L L^{-1}(i_L) A_L^T Q_{CRV} z_e.$$

Lemma 2.2 leads to $A_L^T Q_{CRV} z_e = 0$, i.e.

$$Q_C z_e = Q_{CRV} z_e = 0, \quad (23)$$

since $(A_C A_L A_R A_V)$ has full row rank (see Theorem 1.1). Introducing \bar{Q}_{V-C} as a projector onto $\ker Q_C^T A_V$ we follow from (17) and (21)

$$\begin{aligned} A_C C(A_C^T e) A_C^T z_e + A_V \bar{Q}_{V-C} z_V &= 0, \\ \bar{Q}_{V-C}^T A_V^T z_e &= 0. \end{aligned}$$

Using the fact that

$$\ker \begin{pmatrix} M & N \\ N^T & 0 \end{pmatrix} = \ker M \times \ker N$$

for a positive semidefinite matrix M and any matrix N , this leads to $A_C^T z_e = 0$ and $0 = A_V \bar{Q}_{V-C} z_V = A_V z_V$, which implies $P_C z_e = 0$ and $z_V = 0$, since A_V has full column rank (see Theorem 1.1-2). Together with (23) and (18) we obtain $z = 0$.

q.e.d.

Note, a similar result was presented in [15] for networks consisting of linear resistances, inductances and capacitances as well as constant sources, ideal transformers and gyrators. There, it was shown that the branch voltage - branch current equation system has an index not greater than 2. Furthermore, in [11] it was already proved that the *Tableau Analysis* for networks containing linear capacitances, resistances and voltage sources only provides a DAE index 2 if there is a C-V loop in the circuit.

Theorem 2.3 and Theorem 2.4 permits the application of a number of well-known results about solvability and stability for index-1 and index-2 DAEs (see e.g. [6], [10], [13], [16]). Here, we instance the application of Theorem 4.4. in [13] in order to describe the sensitivity of solutions for DAE systems (3)-(5) with respect to small perturbations. Let us introduce the appropriate solution space $C_N^1 := \{x = (e, j_L, j_V) \in C(\mathcal{I}) : P_C e \in C^1(\mathcal{I}), j_L \in C^1(\mathcal{I})\}$ for a compact interval \mathcal{I} .

Theorem 2.5 *Let the capacitance, inductance and resistance matrices of all capacitances, inductances and resistances, respectively, be positive definite. Given a solution $x_* := (e_*, (j_L)_*, (j_V)_*) \in C_N^1$ of (3)-(5), $t_0 \in \mathcal{I}$. Let $C(A_C^T e)$, $L(j_L)$ be continuously differentiable and $g(A_R^T e)$, $i(t)$, $v(t)$ be twice continuously differentiable.*

(i) *Then, perturbed initial value problems*

$$\begin{aligned} A_C C(A_C^T e) A_C^T e' + A_R g(A_R^T e) + A_L j_L + A_V j_V + A_I i &= \delta_e, \\ L(j_L) j_L' - A_L^T e &= \delta_L, \\ A_V^T e - v &= \delta_V, \\ (e(t_0), j_L(t_0), j_V(t_0)) &= (e_0, (j_L)_0, (j_V)_0) \end{aligned}$$

satisfying

$$Q_C e_0 = Q_C e_*(t_0) \quad \text{and} \quad (j_V)_0 = (j_V)_*(t_0) \quad (24)$$

as well as

$$\bar{Q}_{V-C}^T A_V^T e_0 = \bar{Q}_{V-C}^T A_V^T e_*(t_0) \quad \text{and} \quad Q_{C_{RV}}^T A_L(j_L)_0 = Q_{C_{RV}}^T A_L(j_L)_*(t_0) \quad (25)$$

are uniquely solvable on C_N^1 supposing $|x_0 - x_(t_0)|$ as well as $\|\delta\|_\infty$ (for $\delta := (\delta_e, \delta_L, \delta_V)$), $\|\frac{d}{dt}(Q_{C_{RV}}^T \delta_e)\|_\infty$, $\|\frac{d}{dt}(\bar{Q}_{V-C}^T \delta_V)\|_\infty$ are sufficiently small.*

(ii) *For the solution $x = (e, j_L, j_V)$ of (i) the inequality*

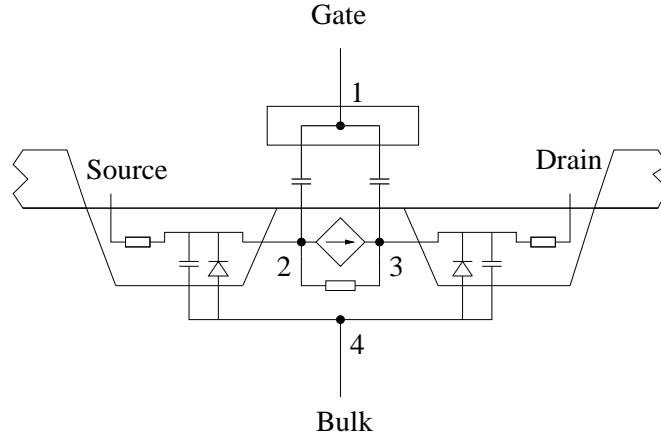
$$\|x - x_*\|_\infty \leq K(\|\delta\|_\infty + \|\frac{d}{dt}(Q_{C_{RV}}^T \delta_e)\|_\infty + \|\frac{d}{dt}(\bar{Q}_{V-C}^T \delta_V)\|_\infty + |x_0 - x_*(t_0)|) \quad (26)$$

is true for a constant $K > 0$.

Remarks:

1. The conditions (24) and (25) guarantee consistent initial values (see [3]). This is useful for implementing a monitor in circuit simulation packages which gives hints to the user about network variables for that he can choose initial values and for which he must not.
2. The inequality (26) implies that $Q_{C_{RV}}^T \delta_e$ and $\bar{Q}_{V-C}^T \delta_V$ reflect the critical defects. This is useful for implementing a monitor in circuit simulation packages which identifies critical parts of the circuit and invokes special treatment for them in order to avoid failures for numerical integration.

3. $Q_{CRV}^T \equiv 0$ iff the circuit does not contain an L-I cut-set (cf. Theorem 1.1-3).
4. $\bar{Q}_{V-C}^T \equiv 0$ iff the circuit does not contain a C-V loop (cf. Theorem 1.1-4).
5. Theorem 2.5 implies that the perturbation index ([10]) coincides with the tractability index for systems (3)-(5).
6. Theorem 2.3 and Theorem 2.4 remain valid if the network contains additionally voltage controlled current sources and each of them satisfy the following condition: The current source belongs to a loop consisting of this source and capacitances only. This fact is important since many networks contain transistor elements, which are often modeled by means of such voltage controlled current sources. For an example, we look at a MOSFET model (cf. [7]):



The current from node 2 to node 3 is controlled by the branch voltages v_{GS} , v_{BS} and v_{DS} . Obviously, the current source belongs to the loop consisting of the source, the capacitance between the nodes 2, 1 and the capacitance between the nodes 1, 3. Hence, Theorem 2.3 and Theorem 2.4 are satisfied for networks containing such MOSFET models.

7. Theorem 2.3 and Theorem 2.4 can also be extended to circuits with other kinds of controlled sources. For a detailed discussion we refer to [5].
8. For networks containing any kind of controlled sources, the index can be greater than 2. A simple example of this is a varactor. For a detailed description of higher index cases see [8].

Finally, look briefly at systems obtained by *charge oriented* MNA:

$$A_C q'_C + A_{RR}(A_R^T e) + A_L j_L + A_V j_V + A_I j = 0, \quad (27)$$

$$\phi'_L - A_L^T e = 0, \quad (28)$$

$$A_V^T e - v = 0, \quad (29)$$

$$q_C = q(A_C^T e), \quad (30)$$

$$\phi_L = \phi(j_L). \quad (31)$$

In comparison with the *classical* MNA, the vector of unknowns consists additionally of the charge of capacitances and of the flux of inductances. Moreover, the original voltage-charge and current-flux equations are added to the system.

Theorem 2.6 *The index of system (27)-(31) coincides with the index of the classical MNA system (3)-(5) for the lower index case (≤ 2).*

Note, $\text{im } A_C = \text{im } A_C q'(A_C^T e) A_C^T$ as well as $\ker A_C^T = \ker A_C q'(A_C^T e) A_C^T$ hold true and ϕ' is regular. Then, following the proof of Theorem 5.6 and 5.7 in [17] we obtain the correctness of Theorem 2.6.

Remarks:

1. Theorem 2.6 implies that Theorem 2.3 and Theorem 2.4 are also valid for DAE systems of the form (27)-(31) obtained by charge oriented MNA.
2. Theorem 2.5 remains valid for systems (27)-(31) if we suppose the conditions

$$(q_C)_0 = (q_C)_*(t_0) \quad \text{and} \quad (\phi_L)_0 = (\phi_L)_*(t_0)$$

to be satisfied, additionally. This follows from considerations in [3] and Theorem 2.5.

3 Summary

Firstly, we have performed an analysis of networks containing general nonlinear but time-independent capacitances, inductances and resistances as well as independent current sources and independent voltage sources. Then, the MNA for such networks has been shown to lead to a DAE-index 1 if and only if the network contains L-I cut-sets or C-V loops. Additionally, the DAE-index for these equation systems has been proved to be not greater than 2. These results are particularly useful when implementing an index monitor in circuit simulation package which identifies critical parts of the circuit to invoke a special treatment for them in order to avoid failures of the numerical integration and gives hints to the user about network variables for which initial values can be chosen.

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